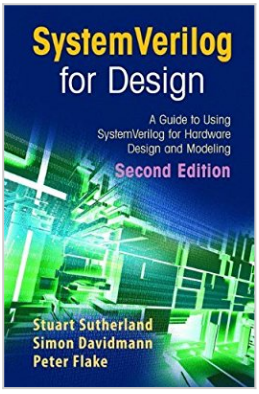

SystemVerilog for Design Second Edition: A Guide to Using SystemVerilog for Hardware Design and Modeling

By Stuart Sutherland, Simon Davidmann, Peter Flake

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In its updated second edition, this book has been extensively revised on a chapter by chapter basis. The book accurately reflects the syntax and semantic changes to the SystemVerilog language standard, making it an essential reference for systems professionals who need the latest version information. In addition, the second edition features a new chapter explaining the SystemVerilog "packages", a new appendix that summarizes the synthesis guidelines presented throughout the book, and all of the code examples have been updated to the final syntax and rerun using the latest version of the Synopsys, Mentor, and Cadance tools.

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Editorial Review

From the Back Cover

SystemVerilog is a rich set of extensions to the Verilog Hardware Description Language (Verilog HDL). SystemVerilog for Design describes the correct usage of these extensions for modeling digital designs. These important extensions enable the representation of complex digital logic in concise, accurate, and reusable hardware models. All key SystemVerilog design features are presented, such as declaration spaces, two-state data types, enumerated types, user-defined types, structures, unions, interfaces, and RTL coding extensions. Emphasis is placed on the proper usage of these enhancements for simulation and synthesis. Design engineers, engineering managers and engineering students working with all sizes and types of digital designs, whether FPGA, ASIC or full custom, will find this book to be an invaluable learning tool and reference guide.

The second edition of this book reflects the official IEEE 1800-2005 SystemVerilog standard. This IEEE SystemVerilog standard adds new capabilities, clarifications, and changes to the Accellera 3.1 SystemVerilog upon which the first edition of this book was based.

Significant updates and revisions in the new edition include:

A new chapter showing how to use SystemVerilog packages with single-file and multi-file compilers.

- New code examples illustrating correct usage of the IEEE version of SystemVerilog.

- Updated coding guidelines reflecting the capabilities of current simulator and synthesis Electronic Design Automation tools such as digital simulators and synthesis compilers.

"SystemVerilog makes it easier to produce more efficient and concise descriptions of complex hardware designs. The authors of this book have been involved with the development of the language from the beginning, and who is better to learn from than those involved from day one?"

? Greg Spirakis, Vice President of Design Technology

Intel Corporation

"Sun has been a driving force in SystemVerilog from its inception. SystemVerilog can significantly improve the productivity of designers in the coming years, and this book is a comprehensive reference text for engineers who want to learn about SystemVerilog for their next generation designs."

? Sunil Joshi, Vice President of Software Technologies & Compute Resources

Sun Microsystems, Inc.

"SystemVerilog addresses the need for efficient and powerful modeling essential to support the complexity, size and scale of next generation hardware designs. This book explains how to use SystemVerilog effectively and provides numerous examples to illustrate how each of the language constructs can best be utilized."

? Chris Malachowsky, Co-Founder and Vice President of Hardware

NVIDIA Corp.

Users Review

From reader reviews:

Mary Gillon:

What do you with regards to book? It is not important to you? Or just adding material when you need something to explain what yours problem? How about your spare time? Or are you busy person? If you don't have spare time to try and do others business, it is give you a sense of feeling bored faster. And you have extra time? What did you do? Every person has many questions above. They should answer that question since just their can do which. It said that about publication. Book is familiar on every person. Yes, it is appropriate. Because start from on pre-school until university need this SystemVerilog for Design Second Edition: A Guide to Using SystemVerilog for Hardware Design and Modeling to read.

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A lot of people always spent all their free time to vacation as well as go to the outside with them family or their friend. Do you know? Many a lot of people spent many people free time just watching TV, or perhaps playing video games all day long. If you wish to try to find a new activity that is look different you can read a new book. It is really fun for you. If you enjoy the book that you simply read you can spent the entire day to reading a guide. The book SystemVerilog for Design Second Edition: A Guide to Using SystemVerilog for Hardware Design and Modeling it is extremely good to read. There are a lot of people that recommended this book. These were enjoying reading this book. Should you did not have enough space bringing this book you can buy the particular e-book. You can m0ore easily to read this book from the smart phone. The price is not to cover but this book provides high quality.

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